REMARKS

In the Office Action, the Examiner rejected claims 1-3 under § 102 as being anticipated by USP 6,546,540 issued to Igarashi et al (Igarashi). The Examiner rejected claims 4-8 and 10-12 under § 103 as being unpatentable over Igarashi in view of USP 5,822,214 issued to Rostoker et al. (Rostoker). The Examiner rejected claim 9 under § 103 as being unpatentable over Igarashi in view of USP 6,680,150 issued to Blatchford et al. (Blatchford). In this Amendment, Applicants have amended claims 1-3. No claims have been cancelled or added. Accordingly, claims 1-12 will be pending after entry of this Amendment.

I. Claims 1-3

The Examiner rejected claim 1 under § 102 as being unpatentable over Igarashi.

Claims 2 and 3 are dependent on claim 1. Claim 1 recites an integrated-circuit ("IC") layout. This IC layout has a first set of vias that have a diamond shape. Each via in the first set of vias traverses at least two layers of the IC layout and has a contact on each of the layers. Each contact is in the shape of a diamond. The layout also has a first set of interconnect lines. Each interconnect line in the first set has an end that has a shape of a partial polygon and terminates on at least one diamond-shaped contact. The polygon has more than four sides.

Applicants respectfully submit that Igarashi does not disclose, teach, or even suggest such an IC layout. Specifically, Applicants respectfully submit that Igarashi does not disclose an IC layout that has:

- a first set of vias that have a diamond shape, where each via in the first set of vias traverses at least two layers of the IC layout and has a contact on each of the layers, where each contact is in the shape of a diamond; and
- a first set of interconnect lines where each interconnect line in the first set has an end that has a shape of a partial polygon and terminates on at least one diamond-shaped contact, where the polygon has more than four sides.

As claims 2 and 3 are dependent on independent claim 1, Applicants respectfully submit that claims 2 and 3 are patentable over Igarashi for at least the same reasons. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims 1-3.

II. Claims 4-8 and 10-12

The Examiner rejected claims 4-8 and 10-12 under § 103 as being unpatentable over Igarashi in view of Rostoker.

Claims 5-8 and 10-12 are dependent directly on independent claim 4. Claim 4 recites an integrated-circuit ("IC") layout. This IC layout has a first set of vias. Each via in the first set traverses at least two layers and has one contact on each of the layers. One of the contacts is in the shape of a rectangle and one of the contacts is in the shape of a diamond. The layout also has a first set of interconnect lines terminating on several of the first set of vias. The interconnect lines in the first set of interconnect lines have ends that terminate on the contacts. Several of the interconnect lines ends are in the shape of a half polygon, where the polygon has more than four sides.

Applicants respectfully submit that the cited references, neither separately nor through their piecemeal hindsight combination, disclose, teach, or even suggest such an IC layout. Specifically, Applicants respectfully submit that the cited references do not disclose an IC layout that has:

- a first set of vias, where each via in the first set traverses at least two layers and has one contact on each of the layers, where one of the contacts is in the shape of a rectangle and one of the contacts is in the shape of a diamond; and
- a first set of interconnect lines terminating on at least several of the first set of vias, where the interconnect lines in the first set of interconnect lines have ends that terminate on the contacts, where several of the interconnect lines ends are in the shape of a half polygon, where the polygon has more than four sides.

The Examiner identified Figures 111 and 131, column 20 lines 49-54, column 57 lines 13-17, column 86 lines 22-38 and lines 49-58 of Rostoker as disclosing the interconnect lines element of claim 4. However, these passages of Rostoker disclose wire ends in the shape of a half rectangle. A rectangle is a polygon that has four sides. Therefore, Applicants respectfully submit that Rostoker does not disclose, teach or even suggest the recited IC layout of claim 4 that has interconnect lines ends in the shape of a half polygon, where the polygon has more than four sides.

As claims 5-8 and 10-12 are dependent on independent claim 4, Applicants respectfully submit that claims 5-8 and 10-12 are patentable over the cited references for at least the same reasons. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claims 4-8 and 10-12.

III. Claim 9

The Examiner rejected claim 9 under § 103 as being unpatentable over Igarashi in view of Blatchford.

Claim 9 recites an integrated-circuit ("IC") layout. This IC layout has a first set of vias, where each via in the first set traverses at least two layers and has one contact on each of the layers. One of the contacts is in the shape of a quadrilateral polygon and one of the contacts is in the shape of a non-quadrilateral polygon.

Applicants respectfully submit that the cited references, neither separately nor through their piecemeal hindsight combination disclose, teach, or even suggest such an IC layout. Specifically, Applicants respectfully submit that the cited references do not disclose an IC layout which has a via that traverses at least two layers and has one contact on each of the layers, where one of the contacts is in the shape of a quadrilateral polygon and one of the contacts is in the shape of a non-quadrilateral polygon.

The Examiner accurately noted that Igarashi does not teach a via that has one of its contacts in the shape of a quadrilateral polygon and one of its contacts in the shape of a non-quadrilateral polygon. The Examiner then cited Figures 1, 3, and 5, and column 2 lines 30-35 of Blatchford as disclosing vias having one contact in the shape of a non-quadrilateral polygon. Applicants respectfully disagree with this characterization of the referenced passages of Blatchford. These passages relate to contact structures which are non-rectangular apertures for forming contact openings on semi-conductor substrates, not to vias. Hence, Applicants respectfully submit that Blatchford does not disclose, teach, or even suggest a via that has one of its contacts in the shape of a non-quadrilateral polygon.

In addition, Applicants respectfully submit that there is no motivation or suggestion to combine the teachings of Blatchford with Igarashi. The mere fact that references can be combined or modified does not render the resultant combination obvious, unless the prior art also suggests the desirability of the combination. Nothing in Igarashi or Blatchford teaches or suggests combining the teachings of their respective disclosures.

Accordingly, Applicants respectfully submit that the cited references, neither separately nor through their piecemeal hindsight combination, disclose, teach, or even suggest such an IC layout which has a via that traverses at least two layers and has one contact on each of the layers, where one of the contacts is in the shape of a quadrilateral polygon and one of the contacts is in the shape of a non-quadrilateral polygon. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 103 rejection of claim 9.

CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 4-14, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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